

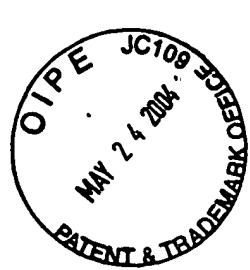
The diagram illustrates the architecture of a memory system, divided into two main functional blocks by a dashed line.

Top Block (Memory Array and Control Logic):

- Memory Cell Array (102):** The central component for storing data.
- Row Control (106):** Manages the selection of rows in the memory array. It receives **WLs** (Word Lines) and sends **control lines** to the **command circuits** and **state machine**.
- Column Control (124):** Manages the selection of columns in the memory array. It receives **BLs** (Bit Lines) and sends **control lines** to the **command circuits** and **state machine**.
- Data I/O (122):** Handles the transfer of data between the memory array and the controller. It receives **I/O data lines** from the controller and sends **control lines** to the **command circuits** and **state machine**.
- Control Circuits (114) and State Machine (116):** These blocks manage the overall operation of the memory array. They receive **control lines** from the controller and send **control lines** to the **row control**, **column control**, and **data I/O** blocks.
- p-well control (108) and c-source control (110):** These blocks manage the p-well and c-source voltages, respectively. They receive **control lines** from the controller and send **control lines** to the **memory cell array**.

Bottom Block (Controller):

- Controller (138):** The central management unit. It contains **RAM (130)** and **ROM (132)**.
- to/from host:** The interface for data transfer between the controller and the host.
- address lines:** Sent from the controller to the **row control** and **column control** blocks.
- I/O data lines:** Sent from the controller to the **data I/O** block.



Title: METHOD OF READING NAND MEMORY TO COMPENSATE FOR COUPLING BETWEEN STORAGE ELEMENTS
Applicant: Chen
Docket No.: SAND-01010US0
Appl. No.: 10/765,693
Atty: Larry E. Vierra
Filing Date: January 26, 2004
Phone: (415) 369-9660

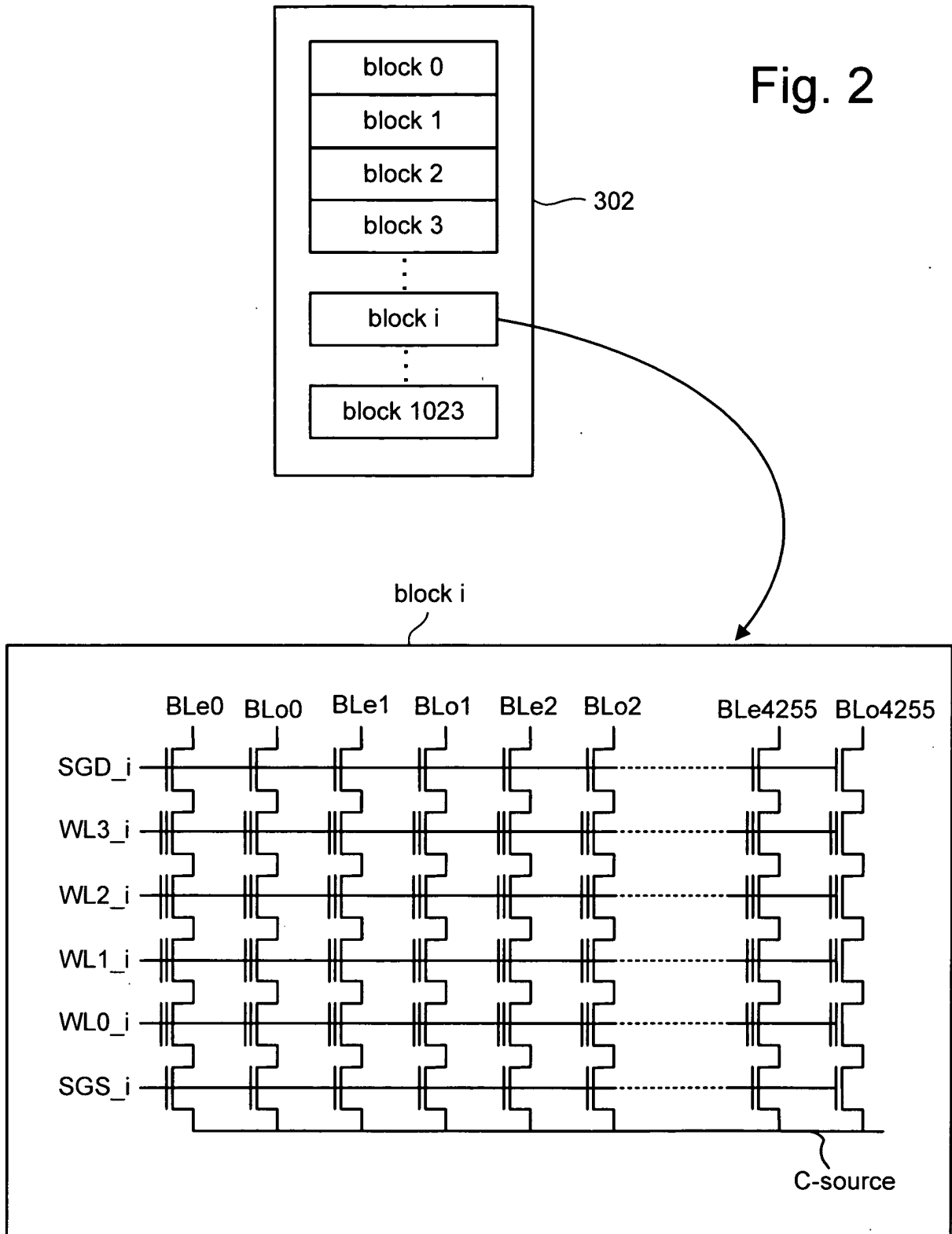


Fig. 3

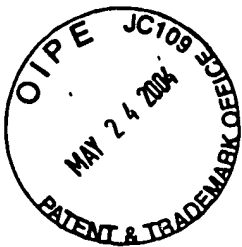


Fig. 4

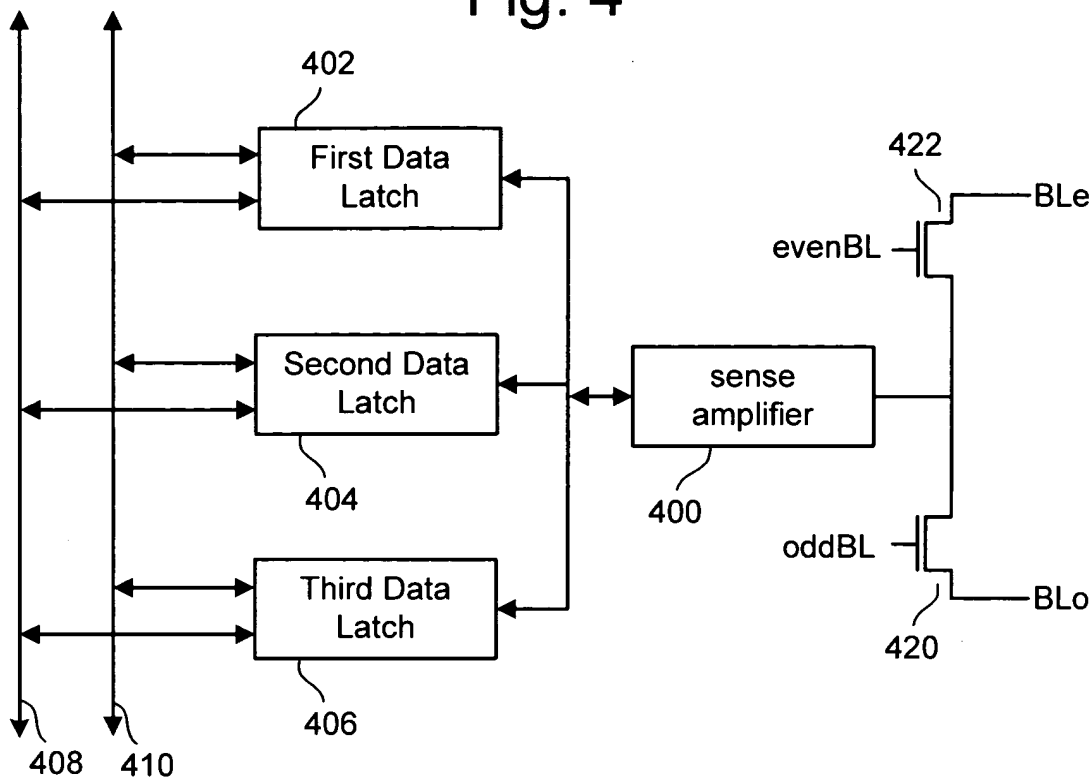
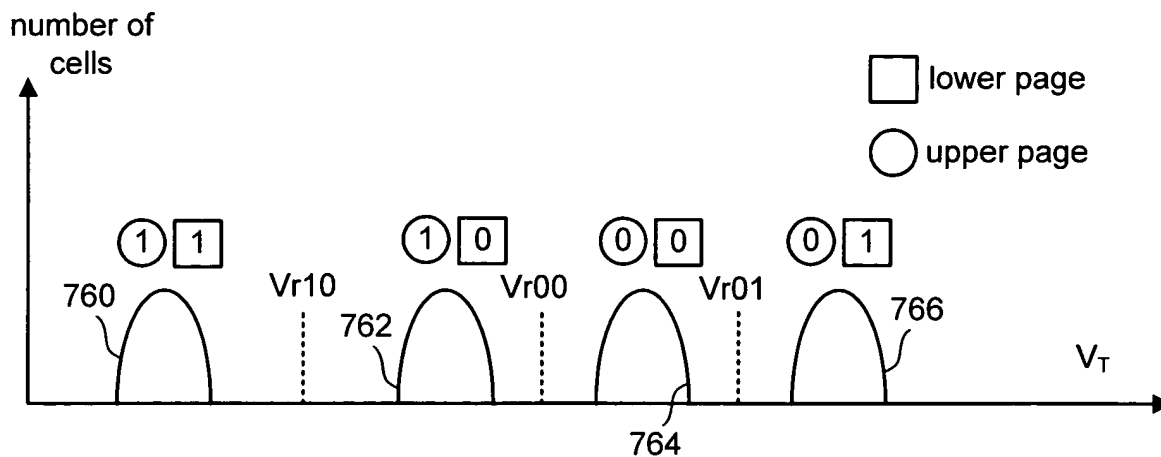


Fig. 5



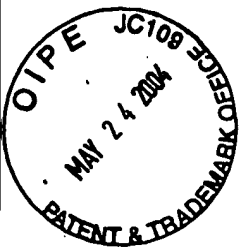


Fig. 6a

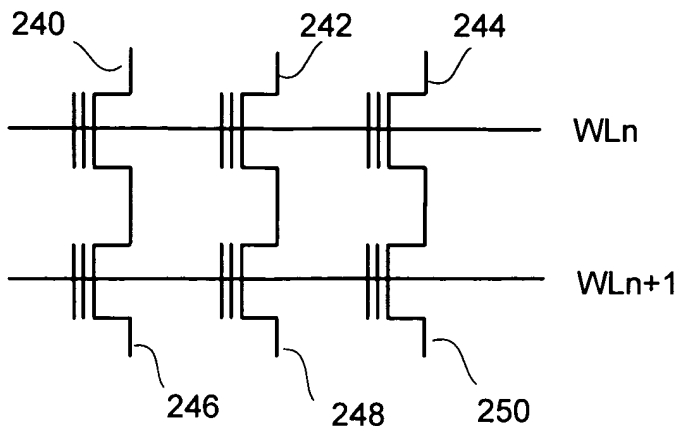


Fig. 6b

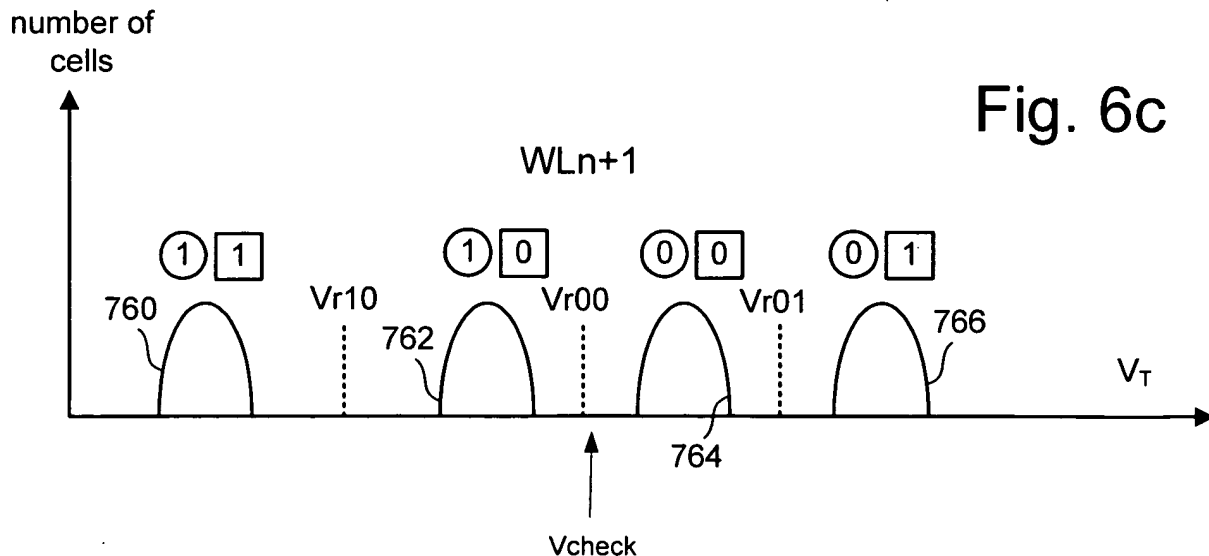
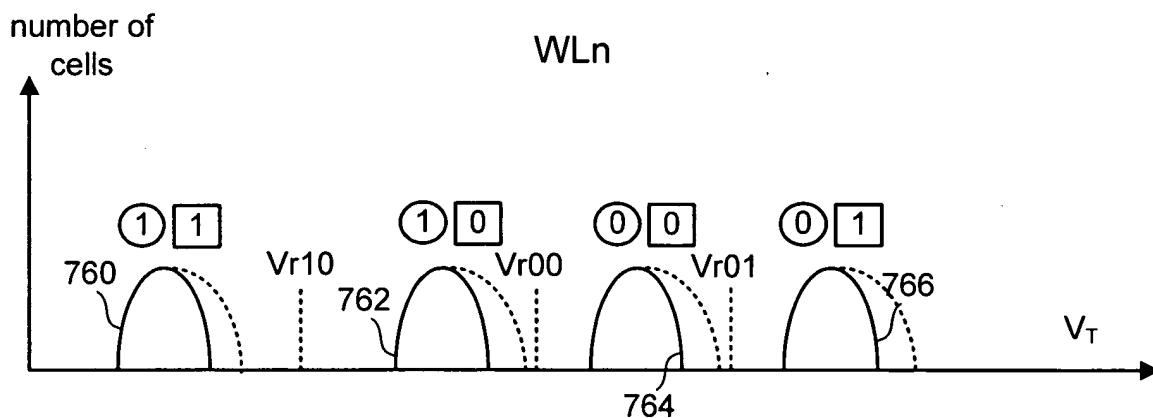
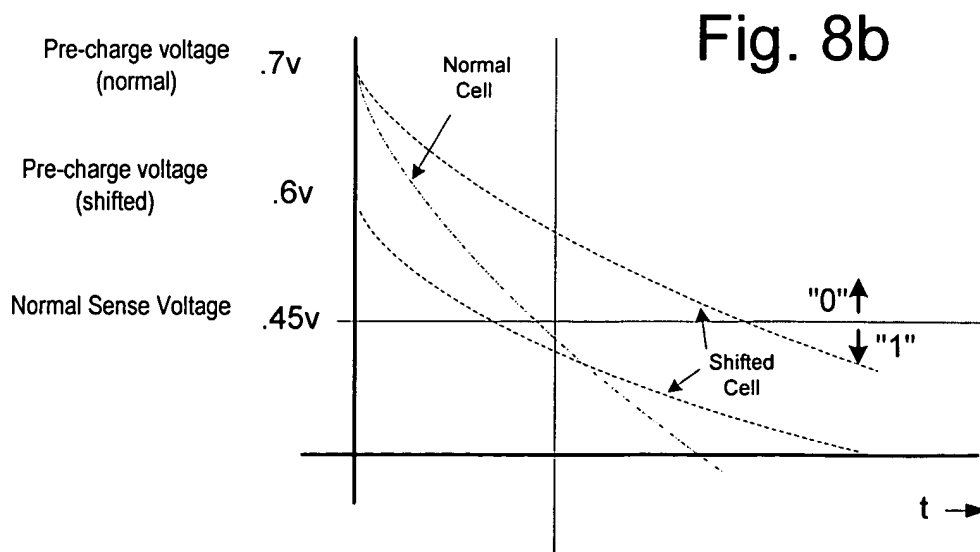
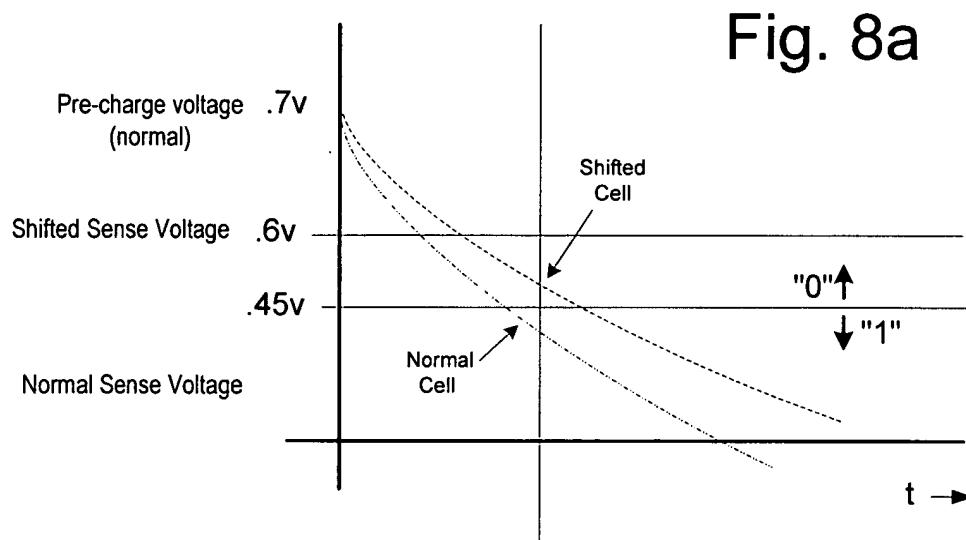
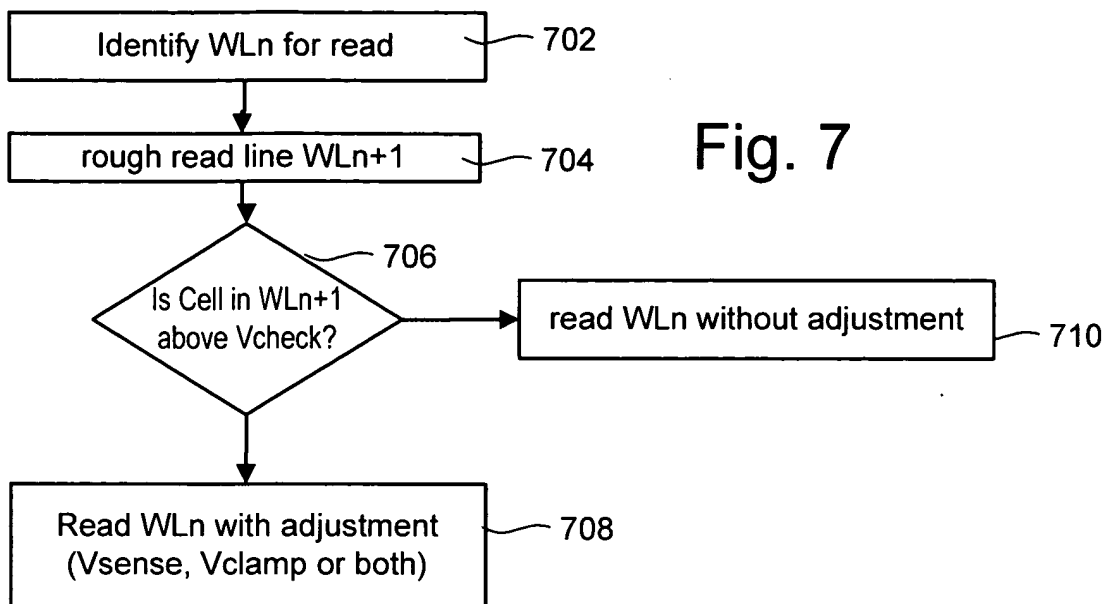
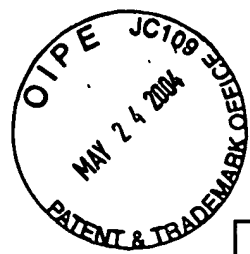


Fig. 6c



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Fig. 9

number of
cells

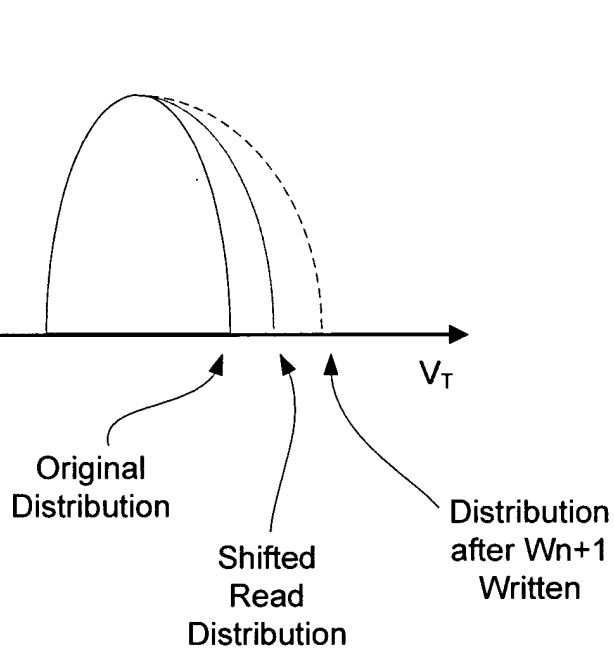


Figure 10b is a semi-logarithmic plot showing the relationship between conductance (G) and voltage (V). The y-axis represents conductance on a logarithmic scale from 10^1 to 10^4 . The x-axis represents voltage, with specific markers for V_{r00} and V_{r01} . Three bell-shaped curves are plotted, corresponding to different clamp potentials (V_{Clamp}):

- $V_{\text{Clamp}} - 60\text{mv}$ (dotted line)
- $V_{\text{Clamp}} - 40\text{mv}$ (dash-dot line)
- $V_{\text{Clamp}} - 20\text{mv}$ (dashed line)
- V_{Clamp} (solid line)

The curves show that the conductance peaks at approximately 4×10^3 for all clamp potentials, with the peak voltage shifting slightly towards more negative values as the clamp potential becomes more negative.



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